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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,705	08/10/2001	Afshin D. Momtaz	019717-002400US	5861

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EXAMINER	
HSU, ALPUS	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/927,705	MOMTAZ, AFSHIN D.	
	Examiner	Art Unit	
	Alpus H. Hsu	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter since claims 9-36 were directed to circuits for performing a line loop back test starting from a serializer to a first-in-first-out buffer to a loop back data multiplexer, and then a deserializer which is contradictory to the claimed invention as disclosed in the specification disclosure which is directed to a circuit for performing a line loop back test starting from a deserializer to a loop back data multiplexer, to a first-in-first-out buffer, and then a serializer.

3. Claims 1-44 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The features of method and circuitry for performing a line loop back test in line loop back mode are critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

The features of method and circuitry for performing a line loop back test includes a receiver, a deserializer, and a low speed parallel loop back data multiplexer selects either the low speed parallel data from the deserializer when in loop back mode or low speed parallel input data when in normal mode. The desedalizer produces a low speed clock output signal that is fed to a low speed loop back reference clock multiplexer and also to a low speed loop back clock multiplexer. Both the loop back reference clock multiplexer and the loop back clock multiplexer select the low speed clock output signal from the deserializer when in line loop back mode. A clock multiplying unit converts the output of the low speed loop back reference clock multiplexer into a high speed clock signal. The serializer generates the high speed serial transmitter data in synchronization with the high speed clock signal received from a clock multiplying unit are critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. To be more specific, all claims were directed to method and circuit for performing line loop back test with method steps or functions performed by each element. But the operation of the line loop back test during the line loop back mode was not clearly recited in the claim to show how the line loop back test can be carried out using the recited method steps or elements.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1 and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by DUCAROIR et al. in Pub. No. US 2001/0043648 A1.

Referring to claims 1 and 37, DUCAROIR et al. discloses a circuit and method for performing a line loop back test, the circuit comprising: a receiver (22) that receives an input signal from a receiver communication line; a desedalizer (24) coupled to the receiver that converts high speed serial receiver data derived from an input signal received by the receiver into low speed parallel data; a low speed parallel loop back data multiplexer (16 and 28) coupled to the deserializer that selects either the low speed parallel data from the deserializer or low speed parallel input data; a serializer (18) coupled to the low speed parallel loop back data multiplexer that converts low speed parallel output data from the low speed parallel loop back data multiplexer into high speed serial transmitter data; and a transmitter (20) coupled to the serializer that converts the high speed serial transmitter data into an output signal for transmission across a transmitter communication line.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5, 8, 41 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over DUCAROIR et al. in Pub. No. US 2001/0043648 A1 in view of RAMAMURTHY et al. in U.S. Patent No. 5,787,114.

Referring to claims 5, 8, 41 and 44, DUCAROIR et al. differs from the claims, in that, it fails to disclose the features of including a low speed parallel loop back data buffer that provides

coupling between the deserializer and the low speed parallel loop back data multiplexer and a clock and data recovery unit that provides coupling between the receiver and the desedalizer, which are well known in the art and commonly applied in data communications field for data buffering and clock and data recovery purposes. RAMAMURTHY et al., for example, from the similar field of endeavor, teaches the uses of a low speed parallel loop back data buffer (16) that provides coupling between the deserializer and the low speed parallel loop back data multiplexer and a clock and data recovery unit (17) that provides coupling between the receiver and the desedalizer, which can be easily adopted by one of ordinary skill in the art to implement into the system of DUCAROIR et al. to further improve the data transmission efficiency.

8. No prior art rejection can be applied to claims 9-36 since the claims were directed to the invention which was not described in the specification disclosure.

9. Claims 2-4, 6, 7, 38-40, 42 and 43 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Drewlo, Staab et al. '124 & '633, Ducaroir et al. '370, Prentice et al., Bonneauet al., and Enam et al. are all cited to show the common feature of line loop back testing utilizing serializer, multiplexers, buffers, and deserializer similar to the claimed invention.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alpus H. Hsu whose telephone number is (571)272-3146. The examiner can normally be reached on M-F (5:30-3:00) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D. Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AHH

Alpus H. Hsu
Primary Examiner
Art Unit 2665